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Feedback TI Confidential—NDA
Restrictions Release History Release Date
Description/Comments D+++ January
2012 • Added Navigator Cloud note to Rx
Flows. (Page 4-23) • Updated QMn Base
Address Regs (Page 4-19)

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KeyStone Architecture Multicore
Navigator User's Guide Literature
Number: SPRUGR9H November
2010—Revised April 2015

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mail.trempealeau.net Definition. •

Multicore Navigator is a collection of hardware components that facilitate data movement and multi-core control. • The major components within the Navigator domain are: – A hardware Queue Manager (QM). – Specialized

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My knowledge about Multicore Navigator is mostly limited with the Multicore Navigator for Dummies and user guide documents. So I have a couple of

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questions: 1) Is it possible to use Multicore Navigator for a complete infrastructure communication in a complete asymmetric system? If yes, I understand that we need to use QMSS TX queues and ...

~~[Resolved] Multicore Navigator for Complete Infrastructure ...~~

Multicore Navigator Question. Intellectual 2025 points Hector Rivera ...

~~Multicore Navigator Question - Processors forum ...~~

i have c6670 multicore messageQ example program its used for 4 cores. 1.how can i restrict into 2 core. 2.what are all the configuration changes in that example code ?

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Since the Packet DMA uses the queue manager, it is assumed that you understand the concepts presented in Part 2 of the Multicore Navigator training. First we will discuss how the Packet DMA works. We'll talk about triggering, transmit processing, receive processing, and infrastructure processing.

~~KeyStone I training: multicore navigator—packet DMA...~~

- Multicore Navigator User Guide (for Packet DMA) PKTDMA Controller SA PA GbE Switch Subsystem INTD Packet Streaming Switch Configuration Bus SGMII0 SGMII1 PHY stat_pend_raw[1:0] misc_int buf_starve_intr mdio_link_intr[1:0] mdio_user_intr[1:0] PKTDMA.

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Multicore Navigator User Guide - Texas Instruments multicore navigator: packet dma (pktdma) ... And you can see all the specific fields by looking at these registers in the Navigator User Guide. And lastly, for the receive DMA, the last register to be configured are the channel control registers.

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